Computer Architecture
PhD Qualifier Exam Examples

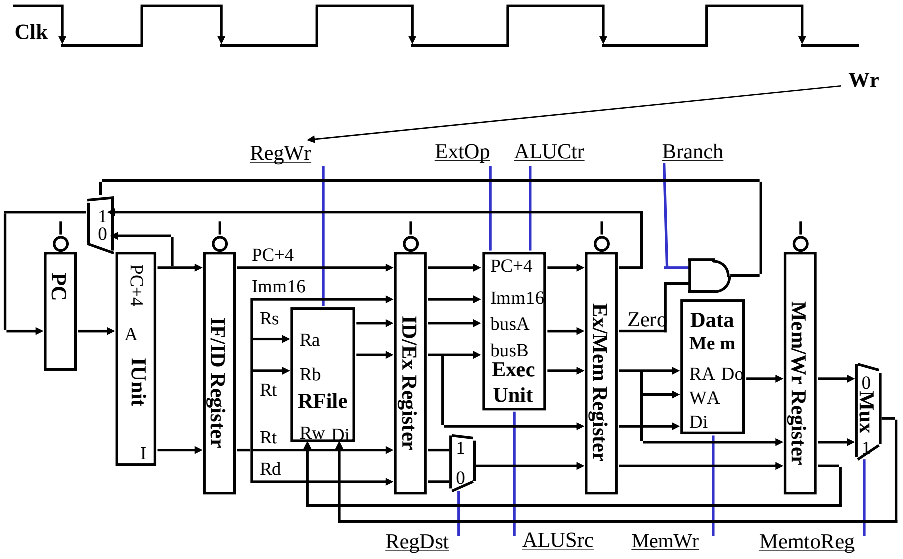
Problem (Pipeling Datapath & Control):

Figure 1 illustrates a 5-stage MIPS pipeline datapath. One *Load*, *R-type (ALU)*, *Store*, *Beq* instruction enters the datapath in Cycle 1, 2, 3, and 4, respectively. Suppose each instruction takes all 5 pipelining stages, i.e., Instruction fetch (IF), Instruction decoding / register fetch (ID/RF), ALU execution (Exec), memory access (Mem), and Register write-back (Wr). Assume there is neither control hazard nor data hazard.

a) Please set the control values in the following table in the end of Cycle 4, 5, and 6, respectively.

	RegDst	RegWr	ExtOp	ALUCtr	MemWr	MemtoReg	Branch
Cycle 4							
Cycle 5							
Cycle 6							

Figure 1: A Pipelined Datapath



Consider the following piece of codes on the pipelining machine.

```
Lw  $1, 100 ($2)
Add $3, $5, $1
Sub  $4, $5, $6
Add $7, $1, $4
Sub  $8, $9, $7
```

b) Assuming there is neither forwarding logics inside the CPU nor compiler help, please draw a diagram with the five pipelining stages to show all of the data hazards. And, how many *no*p instructions need to be inserted?

c) Assuming there are forwarding logics inside the CPU, draw a diagram to show how many data hazards can be resolved, and how many are still there.

d) With the forwarding logics inside the CPU, is it possible to reorder (schedule) the instruction sequence so as to remove data hazards to zero? If yes, show your instruction order?

Problem (Memory Hierarchy):

a) A cache system takes advantage of locality to reduce the average access time to the main memory. The principle of Locality states the programs access a small portion of address space at any instant of time.

What are the two types of locality used in building a cache system? And, use the following program code to give a concrete example for each type of locality.

```
i = 0;
Sum = 0;
While (i < 100) {
        Sum += A[i];                    // A and B are two arrays, C is a variable
        B[i] += C;
        i ++;
}
```

b) Given a series of references in memory word addresses: 1, 4, 7, 5, 12, 9, 11, 20, 9, 13, 4, 5. A cache is empty initially.

Show the hits and misses, and the final cache content for a directed mapped cache with a total of 8 one-word blocks, and for a directed mapped cache with a total of 4 two-word blocks, respectively.

c) Assuming a 32-bit memory address and using block size of 2^m bytes, calculate the **total bits** required for a N-way set associative cache with 2^M bytes of data (N = 2^k); M, N, m, k all integers.

d) Assuming an instruction cache miss rate for *gcc* of 2% and a data cache miss rate for *gcc* of 4%. If a machine (M1) has a CPI of 2 if without any memory stalls and the miss penalty is 40 cycles for all kinds of misses, determine how much faster a machine (M2) that runs with a perfect cache that never missed. The instruction mix of *gcc* is given in the following table.

Instruction class	***Frequency***
R-type	50%
Load	20%
Store	16%
Branch	14%

If we double clock rate of M1 so as to get a machine M3, assuming the absolute time (miss penalty) to handle a cache miss does not change, how much faster M3 than M1?

University of Colorado at Colorado Springs

Ph.D. Qualifier Sample Questions

Please be rigorous about any computation you do. You will be graded not only for the correctness of your answers, but also on your clarity. Be *neat*. Partial credit will be given for substantially attempted questions.

1. Consider the following recurrence relations corresponding to two algorithms: A and A'.

$$T(n) = 7\,T\left(\frac{n}{2}\right) + n^2 \quad (1)$$

$$T'(n) = a\,T'\left(\frac{n}{4}\right) + n^2 \quad (2)$$

   What is the largest value of a such that algorithm A' is asymptotically faster than A? Make sure you do your computations as precisely as you can. Don't jump to answers without supporting steps. Used detailed steps for solving any needed recurrences.

2. Assuming that the SAT problem is NP-Complete, show that the 3-CNF-SAT problem is NP-Complete. Please go through all steps one by one.

   Assuming that the CLIQUE problem is NP-Complete, show that the VERTEX-COVER problem is NP-Complete.

Pick any two of the three questions below:

1. For the CFG with the following production rules (Show all steps in each part)

$$S \rightarrow aC \mid ABaD \mid BD; \quad A \rightarrow aAAb \mid a \mid b \mid aC; \quad B \rightarrow abB \mid aD;$$
$$C \rightarrow aCb \mid b \mid aB; \quad D \rightarrow aaD \mid abB$$

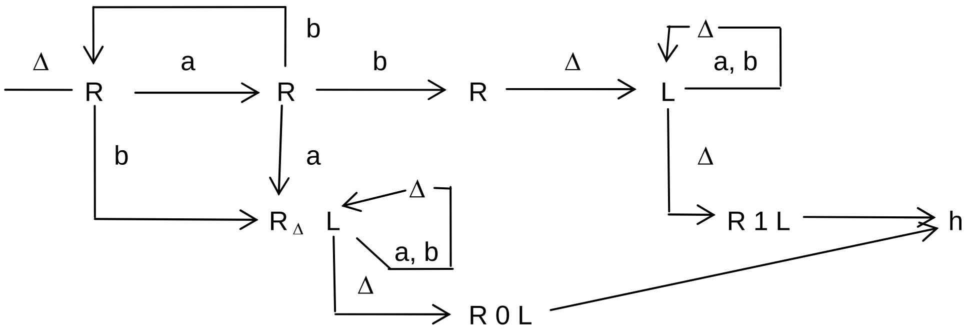
(a) Put the CFG in its simplest form (for human readability) by eliminating all useless variables and production rules.
(b) What set of strings can S derive under closure? Use precise notation.

2. For the language $L = \{ x \mid x \in \{a, b\}^* \mid N_a(x) < N_b(x) \}$, find an accepting PDA.

(a) State the logic you use in constructing the PDA.
(b) Draw the transition diagram.
(c) Include an error state with all error transitions.

3. For the following TM

a) What language L is accepted by the TM? Give your answer in set notation. It must be in simplest form for full credit. Note: Δ is a blank symbol.
b) How would you best characterize exactly what the TM does?



Operating Systems sample questions

Deadlock:

A) Consider a system with 19 disk drives. Each user will never need more than four at a time. Let N be the number of processes. For what values of N is the system deadlock free if we always grant requests for available drives? Why? Does the value of N change if we use a deadlock avoidance algorithm such as, for example, the banker's algorithm to decide whether to grant a request? Why?

B) Terms usually bandied about in the discussion of deadlock include:

Avoidance
Circular Wait
Detection and Recovery
Exclusive Access
Hold and Wait
No Preemption
One Shot Allocation
Prevention
Resource Ordering

Try to group them into categories. Define and explain why you have chosen each of the categories you select.

Scheduling:

A) Suppose your computer uses a multi-level feedback queue to schedule processes. Assume that the queue has the following priority and timeout values and that newly ready-to-run processes enter at priority level 1:

Priority	Time Slice
1	10
2	20
3	40
4	80

Suppose a process repeatedly does 12 ms of computing followed by 10 msec of I/O followed by 35 msec of computing followed by 70 msec of I/O. Describe the path it takes through the scheduler queues.

B) Suppose this system implements a Translation Lookaside Buffer (TLB) and paged page tables in hardware. Suppose that the TLB misses on I % of all virtual memory references, that access to the TLB itself is essentially 0 ns, and that accesses to physical memory take 200 ns. What is the average time required to return data for a virtual memory reference? State any assumptions you make.